UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/728,022	11/30/2000	Thomas W. Williams	SNSY - A2000-001	6107

7590 01/27/2005

SYNOPSY, INC. C/O BEVER, HOFFMAN & HARM
2099 GATEWAY PLACE
SUITE 320
SANJOSE, CA 95110-1017

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/728,022	WILLIAMS ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Oath/Declaration

2. The current Declaration and Power of Attorney form on record as of Nov. 30, 2000 is missing the signature of the inventor Tom Williams.

Drawings

3. Figure 2 is objected to because there are two occurrences of the "Memory1 Mask Memory", one with the number 210 and one without. The "Memory1 Mask Memory" without the reference number (second occurrence) in the lower left corner is not disclosed in the specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because it is over 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claim 7 is objected to because of the following informalities: "In integrated circuit testing ..." should be "An integrated circuit testing ...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 10 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 10 and 17:

Claims recite the limitation "said LFSR". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 6, 7-10, 13-17, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarwala et al. (US-5444716), hereinafter Jarwala.

Claims 1-3, 7-9, 14, 16:

Jarwala teaches a register bank 29 that is coupled via a bidirectional bus 30 to a first memory bank (32) (second memory) and to an automatic test pattern generator 34 (a random number generator). Jarwala teaches the first memory bank 32 is designated as a Test Vector Output (TVO) memory (second memory) because it stores a set of deterministic test vectors for testing the circuit board 12.sub.1 of FIG. 1. Jarwala also teaches the vectors in the TVO memory 32 are generated in advance of testing. Jarwala further teaches the Automatic Test Pattern Generator (ATPG) 34 typically takes the form of a Linear Feedback Shift Register (LFSR per claims 3, 9, and 16) (a random number generator) that generates a separate one of four different patterns of test vectors in accordance with information stored in the Test Vector Manipulation register (based on a seed) within the BSM internal register bank 29. Jarwala even further

teaches the TVO memory 32 (second memory) and the APTG 34 (a random number generator) are coupled to a first and a second input, respectively, of a multiplexer 36 (selector circuit) that passes the signal at a selected one of its first and second inputs to its output, designated as the Test Data Output (TDO) of the BSM 20.sub.1 (coupling to said integrated circuit) which is coupled to a test data input of the chain of Boundary-Scan cells 14.sub.1 -14.sub.p of FIG. 1. (Col. 5, ll. 14-33). Jarwala does not explicitly disclose "a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random". However, Jarwala does disclose a Test Vector Manipulation Register (first memory) that provides the primary test resource control for determining the source of test vectors supplied to the circuit board. Jarwala also discloses this register also determines the destination for responses generated during testing. (Col. 4, ll. 34-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Jarwala's Test Vector Manipulation Register suggests a first memory for storing a mask vector for characterizing corresponding test vector data. The artisan would have been motivated to conclude this because the Test Vector Manipulation Register comprises of memory elements for storing test resource control (mask vector) for determining the source of test vectors supplied to the circuit board (for switching between TVO memory 32 (deterministic test vector data) and the APTG 34 (pseudo random test vector data)).

Claim 6, 13 and 19:

Jarwala teaches the vectors in the TVO memory 32 are generated in advance of testing. (Col. 5, lines 19, 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the vectors generated in advance (deterministic test vector data) that are stored in the TVO memory 32 (second memory) would be generated by an automatic test pattern generator (ATPG) process. The artisan would have been motivated to do so because automatic test pattern generator (ATPG) processes are used for generating deterministic test vector data.

Claim 10:

"an output of said circuit block is coupled to an input of one stage of said LFSR."

Jarwala teaches the responses generated by the circuit board 12.sub.1 of FIG. 1 (circuit block) are also compacted by a Linear Feedback Shift Register 40. (Col. 5, ll. 39-45).

Claim 15:

"e) applying said output test vector to said circuit block;"

Jarwala teaches the TDO output of the BSM 20.sub.1 is coupled to a test data input of the chain of Boundary-Scan cells 14.sub.1 -14.sub.p of FIG. 1. (Col. 5, ll. 31-33).

"f) obtaining an output generated by said circuit block in response to said output test vector;"

Jarwala teaches the TVI memory bank 38 stores responses generated by the chain of Boundary-Scan cells 14.sub.1 -14.sub.p of FIG. 1, in response to test vectors supplied thereto, via the multiplexer 36. (Col. 5, ll. 36-38).

"g) verifying said circuit block by comparing said output generated by said circuit block to a reference output."

Jarwala teaches the BSM 20.sub.1 also includes an interrupt/sample logic circuit 48 coupled to the bus 30 who's function is to facilitate sampling of information generated by the chain of Boundary-Scan cells during testing. (Col. 6, ll. 5-11).

Claim 17:

"applying said output test vector to said circuit block; obtaining an output generated by said circuit block in response to said output test vector;"

These limitations are rejected per claim 15, steps e) and f) above.

"supplying said output generated by said circuit block to an input of a stage of said LFSR."

This limitation are rejected per claim 10 above.

Claim 20:

Jarwala teaches the Boundary-Scan cells 14_1 -14_p each comprise a single-bit register associated with a node of an electronic component 15, such as an integrated circuit or the like. (Col. 3, ll. 8-11).

7. Claims 4, 5, 11, 12, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarwala et al. (US-5444716), hereinafter Jarwala in view of Lesmeister (US-6101622), hereinafter Lesmeister.

Claims 4, 5, 11, 12 and 18:

Jarwala does not explicitly disclose "said mask vector is data compressed" and "a decompressor coupled between said first memory and said selector circuit". However, Jarwala does disclose a Test Vector Manipulation Register (first memory) that provides the primary test resource control for determining the source of test vectors supplied to the circuit board. Lesmeister teaches each DATA value stored in FIFO buffer 28 (first memory) is a compressed version of a set of one or more vectors. Lesmeister also teaches decompressor circuit 30 decompresses each read out DATA word to produce a sequence of one or more vectors which includes an input "mode selection" field (MODE_SEL). (Col. 4, ll. 57, 58, 62, 63, col. 5, ll. 42-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jarwala's Test Vector Manipulation Register (first memory) to include Lesmeister's FIFO buffer 28 (first memory). The artisan would have been motivated to do so because it would enable Jarwala to store compressed data as a mask vector and to save storage capacity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jarwala's internal register bank 29 to incorporate Lesmeister's decompressor circuit 30. The artisan would have been motivated to do so because it would enable Jarwala to decompress Lesmeister's "mode

selection" field (MODE_SEL) from the first memory and provide the decompressed mode select to the selector circuit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Motika et al. (US-5983380)

Motika teaches pseudo random data from an LFSR and deterministic data from a register multiplexed to load scan chains in an integrated circuit. (Claims 1, 7, 14)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100